

DFT calculation for electronic structure of SiC-MOS after NO annealing.

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ABSTRACT

SiC attracts much attention as a channel for the next-generation power devices, but the mobility of the MOS interface is significantly lower than that of bulks. One of the reasons for low carrier mobility is expected to be the interface defects; the steps generated during the fabrication process of SiC are a source of defects. NO annealing is performed after thermal oxidation process to increase the field-effect mobility. To further increase the field-effect mobility, it is indispensable to reveal the behavior of N atoms introduced by the NO annealing. Our previous DFT study has reported that the density of the discontinuities of the conduction band edge states in the inversion layer at the step edges, which prevent carrier from penetrating from the source to drain, is reduced by NO annealing[1]. However, the areal N-atom density was high compared with the experimental situation because of the limitation of computational resources. In this study, we employ the interface structures, in which the areal N atom density is reduced to replicate the real devices accurately, and find that the nitride layers also screen the unfavorable effect from the SiO₂. The carrier scattering at the partially nitride region is also investigated by the electron-transport property calculations based on DFT.

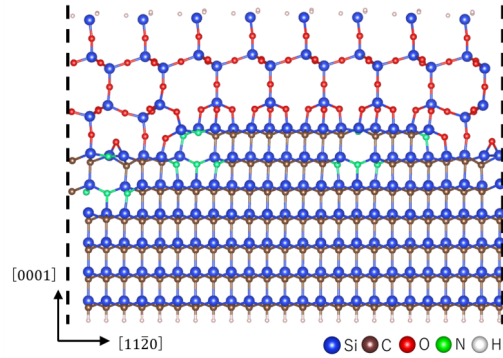


Figure 1: Computational model for interface with step. Dashed lines indicate the boundary of the calculation supercell.

References

- [1] M. Uemoto, N. Funaki, K. Yokota, T. Hosoi, T. Ono, Applied Physics Express, **17**, 011009(2024).